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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TSEGAYE, SABA	
ART UNIT	**PAPER NUMBER**
2662	14

DATE MAILED: 01/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/236,526	KHOURI ET AL.	
	Examiner	Art Unit	
	Saba Tsegaye	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,9-14,16 and 18-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,9-14,16 and 18-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. Claims 1, 7, 9, 10 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art in view or Klecka et al. (6,393,582).

The Admitted prior art discloses a network switch having a processor card including a memory, a stats table, and a routing table that contains the list of current connections. Further, the Admitted prior art discloses reinitializing software, in response to an error that is executed on a networking device card. (page 3)

However, the Admitted prior art does not expressly disclose the following steps: determining if an error is ignorable; determining whether a threshold has been reached if the error is determined to be ignorable, the threshold corresponding to a number of hitless rebuilds that have occurred within an amount of time; and performing a hitless rebuild in the processor card (as in claims 1, 9 and 10); and setting the processing unit to enter into a degraded mode if the error is not ignorable and if the threshold has been reached (as in claims 7 and 16).

Regarding claims 1, 9 and 10, Klecka discloses, in Figs. 1 and 3, a processor card (10) including a memory (20, 30) and a processing unit (12, 14) in the processor card comprising:

detecting an error (steps 52-54);

determining if the error is ignorable (step 56);

determining whether a threshold has been reached if the error is determined tobe ignorable, the threshold corresponding to a number of hitless rebuilds that have occurred within an amount of time (column 2, lines 12-20; column 4, lines 18-39); and

performing a hitless rebuild in the processor card (steps 60-72).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to add a method of steps: that determining if the error is ignorable; determining whether a threshold has been reached if the error is determined to be ignorable; the threshold corresponding to a number of hitless rebuilds that have occurred within an amount of time; and performing a hitless rebuild in the processor card, such as that suggested by Klecka, in the method of the Admitted Prior Art in order to provide a system having soft error recovery capability and, further, to provide a method and apparatus that precludes the logical processor from entering a loop of error detection and recovery from which it cannot escape (column 2, lines 14-19).

Regarding claims 7 and 16, Klecka discloses the method further comprising setting the processing unit to enter into a degraded mode if the error is not ignorable and if the threshold has been reached (column 4, lines 28-34).

It would have been obvious to one ordinary skill in the art at the time the invention was made add a method that sets the processing unit to enter into a degraded mode if the error is not ignorable and if the threshold has been reached, such as that suggested by Klecka, in the method of the Admitted Prior Art in order to provide a method and apparatus that precludes the logical processor from entering a loop of error detection and recovery from which it cannot escape (column 2, lines 14-19).

2. Claims 18, 21-23, 26-28, 31-33, 36-38, 42, 44, 48, 50, 53, 55, 58, 60, 63-65, 68 and 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted prior art (pages 1-4) in view or Hess et al. (US 5,313,625).

The Admitted prior art discloses a network switch having a processor card including a memory, a stats table, and a routing table that contains the list of current connections. Further, the Admitted prior art discloses reinitializing software, in response to an error that is executed on a networking device card.

However, the Admitted Prior Art does not expressly disclose a protected memory region that stores information that can be used by the processor to execute the software and re-initializing not deleting routing table information and state table information (as in claims 18, 23, 28, 33, 38, 44, 50, 55, 60 and 65) and protected memory region further comprises a segment of random access memory (as in claims 21, 22, 26, 27, 31, 32, 36, 37, 42, 48, 53, 58, 63, 64, 68 and 69).

Regarding claims 18, 23, 28, 33, 38, 44, 50, 55, 60 and 65, Hess teaches, in Fig. 1, protected memory means for storing system data, including the state variables, program status words, other critical data and the like (as a function of the system), i.e., data which contains that information which would enable the system to recover from correctable faults. The protected area data provides the system re-initialization state for rapid restart of the digital processor data processing cycle.

It would have been obvious to one ordinary skill in the art at the time of the invention was made to add a protected memory region to store state table information that can be used by the processor to execute the software after software has been reinitialized, such as that suggested

by Hess, in the memory of the Admitted Prior art in order to provide a system having soft error recovery capability.

Neither reference explicitly states that the protected memory stores routing table information (as in claims 18, 28, 38 and 50), status of an interface card located within the networking hardware apparatus (as in claims 23, 33 and 55) and network topology information (as in claims 60 and 65).

However the memory of processing unit could be modified to store routing table information, status of the interface card and the topology information since Hess teaches the protected memory that stores system data, including the state variables, other critical data a function of the system, i.e., data which contains that information which would enable the system to recover from correctable faults.

Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention was made to add a modified protected memory that stores information, such as that suggested by Hess, in the memory of the Admitted Prior Art in order provide a system that minimize the amount of time for rearranging or restructuring of the state information, topology information and routing tables due to resetting of the system.

Regarding claims 21, 22, 26, 27, 31, 32, 36, 37, 42, 48, 53, 58, 63, 64, 68 and 69, Hess teaches that data is written, during normal operation of DPUs, into the scratchpad RAM1 and RAM 2 portion of protected area 4 (column 4, lines 48-65).

It would have been obvious to one ordinary skill in the art at the time of the invention was made to add random access memory, such as that suggested by Hess, in the memory of the

Admitted Prior Art in order to provide a memory that shared by another program or by an interrupt service routine.

3. Claims 2-5 and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art in view of Klecka as applied to claim 1 above, and further in view of Hess et al. '625.

The Admitted Prior Art in view of Klecka discloses all the claim limitations as stated above except for a protected memory region (as in claims 2 and 11); a protecting a memory contains a set of memory addresses (as in claims 5 and 14) and a set of state tables (as in claims 4 and 13).

Regarding claims 2, 4, 5, 11, 13 and 14, Hess teaches, in Fig. 1, protected memory means for storing system data, including the state variables (as in claims 4 and 13), program status words, other critical data and the like (as a function of the system), i.e., data which contains that information which would enable the system to recover from correctable faults (as in claims 5 and 14). The protected area data provides the system re-initialization state for rapid restart of the digital processor data processing cycle (column 4, lines 43-65) (as in claims 2 and 11). Further, Hess teaches that if the processing disruption, continues to persist and causes further cycling through the vector to re-initialize and restart, after an appropriate number of processing resumption attempts, the digital processor would be disabled in an appropriate manner (column 6, lines 25-67).

It would have been obvious to one ordinary skill in the art at the time the invention was made to add a protected memory, such as that suggested by Hess, in the system of the Admitted

Prior Art in view of Klecka in order to provide a system that stores system data in the protected memory which is immune from transient conditions.

Regarding claims 3 and 12, neither reference states a portion of the memory that contains a set of routing tables.

However, it would have been obvious to one ordinary skill in the art at the time the invention was made to store a set of routing tables in the protected memory in order to provide reliable information, which permits the system to determine the outgoing link to be used to forward the packet to the appropriate destination.

4. Claims 19, 20, 24, 25, 29, 30, 34, 35, 39-41, 45-47, 51, 52, 56, 57, 61, 62, 66 and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted prior art in view of Hess as applied to claims 18, 23, 28, 33, 38, 44, 50, and 55 above, and further in view of Rakavy et al. (US 6,324,644).

The Admitted Prior art in view of Hess discloses all the claim limitations as stated above. Further, Hess teaches that data is written, during normal operation of DPUs, into the scratchpad RAM1 and RAM 2 portion of protected area 4.

However, the Admitted Prior art in view of Hess does not expressly disclose non-volatile memory and volatile memory.

Rakavy teaches, in Fig. 2, a non-volatile memory 125, volatile memory and random access memory 120. Further, Rakavy teaches that the non-volatile memory does not change state when the computer is reset.

It would have been obvious to one ordinary skill in the art at the time of the invention was made to substitute non-volatile memory and volatile memory, such as that suggested by Rakavy, the memory of the Admitted prior art in view of Hess in order to provide a memory that shared by another program or by an interrupt service routine.

5. Claims 43, 49, 54 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted prior art in view of Hess as applied to claims 18, 23, 28, 33, 38, 44, 50, and 55 above, and further in view of Treu (US 5,245,615).

The Admitted prior art in view of Hess discloses all the claim limitation as stated above except for dynamic random access memory.

Note that dynamic random access memories are more commonly used than RAMs because dynamic random memory is less expensive than static RAM and their circuitry is simpler.

True teaches that random access memory comprises dynamic random access memory (column 2, lines 65-67).

It would have been obvious to one ordinary skill in the art at the time the invention was made to use dynamic RAM, such as that suggested by True, in the memory of the Admitted prior art in view of Hess in order to provide less expensive memory.

Response to Arguments

6. Applicant's arguments with respect to claims 1-5, 7, 9-14, 16 and 18-69 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saba Tsegaye whose telephone number is (703) 308-4754. The examiner can normally be reached on Monday-Friday (7:30-5:00), First Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (703) 305-4744. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-0377.

ST

January 6, 2004

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